CLAIMS

7. A Mask configurable Smart Power IC to provide switching power cells, their drives and protections and other required circuits to control, amplify and sample output variables, the versatility of which is designed to meet a wide range of requirements and the said Smart Power IC is characterized by:

a) comprising Arrays aimed at Power Integrated Circuits (PICs), based on the association of NMOS FETs, wherein said, NMOS structures, using a specific layout in a simple pattern, enabling to perform, by mask configuration of the top metal layers, the different functions required by Smart Power ICs;

b) providing circuit Topologies to enable the control and power signals processing of PICs resorting only to wherein said NMOS structures in association with passive components within the same monolithic circuit or external to it;

c) using wherein said NMOS based Basic Cells, which make use of an association of FETs, such as LDD or LDSD-NMOS or both, or LDMOS or N channel DMOS.

8. A Mask configurable Smart Power IC as defined in claim 7 implemented by wherein said Programmable Smart Power Arrays by means of:

a) complete mask layout to define the NMOS based elementary associations, that support system built-up;

b) Topologies of the circuits aimed at power signals processing specific functions required by PIC, using wherein said NMOS structures associations , to be added in Cell libraries, in order to be used towards a wide range of applications; and

c) top metal masks layout, which define the semi-custom arrays NMOS structures interconnections, according to the specific topologies of the required circuits.

9. A Mask configurable Smart Power IC as defined in claim 7, the circuits topologies of which are obtained through appropriate configuration of the wherein said Programmable Smart Power Arrays as defined in claim 8 and are required by PICs power control, switching and related drives; sampling and protection., which circuits include:

a) said rectifiers and wherein said programmable "Zeners", required in NMOS based clippers and clampers;

b) wherein said NMOS based level-shifter;

c) wherein said NMOS based charge-pump;

d) wherein said NMOS based bootstrap; and

e) wherein said NMOS based current source;

and appropriate design methodologies and simulation models of which were developed.

10. A Mask Configurable Smart Power IC as defined in claim 1, characterised by elementary associations, only resorting to a set of NMOS transistors either of LDD or LDSD type, or both, or LDMOS or DMOS, which include:

a) flexible interconnection of the whole set of NMOS structures terminals;

b) a P+ guard ring connected to the substrate, involving the elementary cell;

c) connection of LDD type transistors Sources to the referred guard ring;

d) floating LDSD and LDMOS type transistors Sources;

e) specific layout to:

- permit local interconnections of Drain, Gate and Source terminals;

-make easy the implementation of interconnections through columns between the elementary cells; and

- make easy the association of elementary cells in order to obtain more complex circuits.

11. The Mask configurable Smart Power IC Applications resorting exclusively to NMOS based built-in Arrays, as defined in claims 7, 8 and 9, can be fabricated either using standard CMOS technology or other CMOS technologies that require additional process steps or yet sophisticated Power Integration technologies or specific Smart Power technologies, and use top metal mask layout, as defined in claims 8 and 9, according to the methodology defined in claim 10, to select the required functionality making use of the arrays built-in NMOS structures:

- to implement one of a large set of power switching cells presenting different switch topologies – high-side; low-side; pass element; push-pull; half-bridge; full-bridge, n-phases-bridge and other derived topologies;
- to implement required devices and circuits for driving the selected power switching topology;
- to implement required sampling and protection circuits to achieve a good performance of the power switching cells;
- to increase the robustness of smart power ICs with respect to electrostatic discharges and latch-up behaviour;
- to generate reusable cores and power control circuit libraries to be added to the libraries that already exist; and
- to fast prototype Smart Power circuits and Microsystems.

12. Gate-Shifted LDD and LDSD type, N channel, Metal-Oxide-Semicondutor Field Effect Transistors, wherein said Gate-Shifted Lightly Doped Drain - GSLDD and wherein said Gate-Shifted Lightly Doped Source and Drain - GSLDSD, which resort to the wherein said gate-mask shift with respect to N-well mask edge to enlarge breakdown voltage and thus, to expand the application range of wherein said Mask Programmable Smart Power Arrays as defined in

claims 7, 8, 9, 10 and 11, comprising:

- fully standard CMOS (N-well, P substrate, one polysilicon layer and at least two metal layer) compatible;
- a lateral planar configuration for the wherein said GSLDD, with the said Drain formed by a high impurities concentration diffusion embbeded in the low doping concentration N-well;
- a connection between said substrate and said source terminals for the wherein said GSLDD;
- specific mask layout that allows the said GSLDD drain to handle high voltages;
- a lateral planar configuration for the wherein said GSLDSD, with said Drain and Source formed by high impurities concentration diffusions embbeded in low doping concentration N-wells;
- said source and drain terminals isolated from the said substrate for the wherein said GSLDSD;
- specific mask layout that allows both said GSLDSD drain and source to handle high voltages;
- the use of the wherein said gate-shift technique, to obtain the alignment of the said gate mask with the said N-well lateral diffusion periphery path, taking advantage of reduced surface electric field maximum values inherent to low impurities concentration regions, thus increasing device maximum voltage rating.